REMARKS

This amendment responds to the Office Action dated June 5, 2002 in which the Examiner required a new title, objected to the drawings and claims 6 and 10, rejected claims 4-7, 11-16 under 35 U.S.C. § 112, second paragraph, rejected claims 1-4, 6-8, 14 under 35 U.S.C. § 103, stated that claims 5, 11, 12, 15 and 16 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112, second paragraph and stated that claims 9-10 are allowable.

As indicated above, a new title has been provided which clearly indicates the invention to which the claims are directed. It is respectfully requested that the Examiner approves the new title.

Concurrently filed with this Amendment is a Request to Add New Drawings in order to show the different film thicknesses of the gate insulating films. It is respectfully requested that the Examiner withdraws the objection to the drawings.

As indicated above, minor informalities in claims 6 and 10 have been corrected. It is respectfully requested that the Examiner approves the corrections and withdraws the objection to claims 6 and 10.

As indicated above, claims 4, 7, 11, and 13 have been amended in order to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. In particular, typographical errors have been corrected in claims 4, 7, 11 and 13. It is respectfully requested that the Examiner approves the corrections and withdraws the rejection to the claims under 35 U.S.C. § 112, second paragraph.

Claim 1 claims a semiconductor device comprising a gate electrode, first and second diffused layers, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film lying therebetween. The first and second diffused layers are formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each layer has a second conduction type different from the first conduction type of the substrate portion. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and the substrate, and connects the wiring layer to the first diffused layer and the gate electrode.

Through the structure of the claimed invention having a contact connect a wiring layer to the first diffused layer and the gate electrode, as claimed in claim 1, the claimed invention provides a semiconductor device which has an improved soft error resistance. The prior art does not show, teach or suggest a contact connecting a wiring layer to a gate electrode as claimed in claim 1.

Claim 4 claims a semiconductor device comprising a gate electrode, a diffused layer, a wiring layer and a contact. The gate electrode is formed on a substrate through a gate insulating film. The diffused layer is formed on the substrate. The wiring layer is formed above the gate electrode. The contact is formed within a contact hole between the wiring layer and substrate, and connects the wiring layer to the diffused layers and the gate electrode. The diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type. Each of the first and second portions has a second conduction type

different from the first conduction type of the portion of the substrate. A third portion connects the first portion to the second portion.

Through the structure of the claimed invention having a contact which connects the wiring layer to both the diffused layer and the gate electrode, as claimed in claim 4, the claimed invention provides a semiconductor device with an improved soft error resistance. The prior art does not show, teach or suggest a contact connecting a wiring layer to a gate electrode as claimed in claim 4.

Claims 1-4, 6-8 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over *Igarashi et al.* (U.S. Patent No. 6,299,314) in view of prior art Figure 31.

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. § 103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Igarashi et al. appears to disclose in FIG. 20, MOS transistors Q5 and Q6, each being isolated by a STI film ST, are disposed on a silicon substrate 1. A gate structure GT64 is disposed as a gate wiring, on the STI film ST. The MOS transistors Q5 and Q6 have gate structures GT65 and GT66, respectively, and a source/drain layer 7 disposed in the surface of the silicon substrate 1 lying on both sides of the gate structures GT65 and GT66. A salicide layer 61 formed from cobalt salicide is disposed on the surface of the source/drain layer 7. The gate structure GT64 comprises a gate oxide film 2 on the STI film ST, gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, an upper nitride film 4 on the gate electrode 3, and a sidewall nitride film 5

disposed such as to make contact with the side faces of the upper nitride film 4, gate electrode 3 and gate oxide film 2. The gate structure GT65 comprises a gate oxide film 2 on the silicon substrate 1, a gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, an upper nitride film 4 on the gate electrode 3, and a sidewall nitride film 5 disposed such as to make contact with the side faces of the upper nitride film 4, gate electrode 3 and gate oxide film 2. The gate structure GT66 comprises a gate oxide film 2 on the silicon substrate 1, a gate electrode 3 which is formed from polysilicon and disposed on the gate oxide film 2, a salicide layer 6 on the gate electrode 3, and a sidewall nitride film 5 disposed such as to make contact with the side faces of the salicide layer 6, gate electrode 3 and gate oxide film 2. An oxide film 8 and nitride film 9 which are disposed such as to follow the contours of the gate structures GT65 and GT66 remain partially on the upper parts of the gate structure s GT65 and GT66. An interlayer insulating film 10 formed from a silicon oxide film is disposed such as to cover the gate structures GT64 to GT66, including the nitride film 9. A contact hole CH12 for exposing the gate structure GT64 penetrates the interlayer insulating film 10 and reaches the source/drain layers 7 having sandwiched therebetween the STI film ST. A conductor layer CL12 formed from, for example, tungsten is buried in the contact hole CH12, thereby forming the shared contact that connects concurrently the respective source/drain layers 7 of the MOS transistor Q5 and Q6. In the gate structure GT64, since the gate electrode 3 is covered with the nitride film, it can be prevented from being exposed due to the etching of the interlayer insulating film 10, and there is no possibility of being

electrically connected to the respective source/drain layers 7 of the gate structures GT65 and GT66. (col. 20, line 55 through col. 21, line 39)

Thus, *Igarashi et al.* merely discloses that the conductor layer CL12 formed in the contact hole CH12 is in contact with a side wall nitride film 5. Thus, nothing in *Igarashi et al.* shows, teaches or suggests that the contact connects the wiring layer to the gate electrode as claimed in claims 1 and 4 and new claim 17. Rather, *Igarashi et al.* teaches away from the claimed invention since the conductor layer CL12 connects to a side wall nitride film 5.

Figs. 30 and 31 show a well area 10, a diffused layer 20, a gate electrode 30, an interlayer film or dielectric 50, and a common contact hole 60. This common contact hole 60 has a structure in which the gate electrode 30 and the diffused layer 20 corresponding to source/drain are situated at some distance to prevent their overlapping. This is to avoid a problem that the gate electrode 30 and the substrate 10 may be shorted by passing the gate electrode 30 through the thin gate oxide film under the gate electrode when the gate electrode 30 extends onto the silicon substrate. Actually, a sidewall of SiO_2 is provided in an isolation portion between the gate electrode 30 and diffused layer 20 in order to avoid the short between the gate electrode 30 and the substrate. However, this structure is not illustrated in Figs. 30 and 31 for simplicity.

Thus, prior art Figure 31 merely discloses a side wall of SiO_2 provided between the gate electrode 30 and diffused region 20 as well as a contact hole 60. Thus, nothing in the prior art shows, teaches or suggests a contact which connects a wiring layer to the gate

electrode as claimed in claims 1 and 4 and new claim 17. Rather, the prior art merely discloses that the contact hole 60 is in fact in contact with the unshown sidewall.

The combination of *Igarashi et al.* and prior art Figure 31 would merely suggest a contact which connects to a sidewall. Thus, nothing in the combination shows, teaches or suggests a contact which connects a wiring layer to a gate electrode as claimed in claims 1 and 4. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 4 under 35 U.S.C. § 103 and allows new claim 17.

Claims 2-3, 6-8 and 14 depend from claims 1 and 4 and recite additional features. It is respectfully submitted that claims 2-3, 6-8 and 14 would not have been obvious within the meaning of 35 U.S.C. § 103 over *Igarashi et al.* and prior art Figure 31 at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2-3, 6-8 and 14 under 35 U.S.C. § 103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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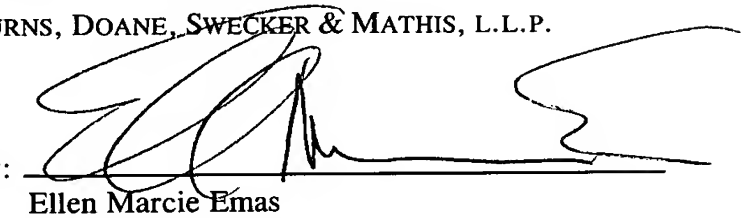

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Paragraphs on Page 7, line 25 through line 30

--Fig. 30 is a plan view showing the structure of a common contact hole of the prior art; [and]

Fig. 31 is a sectional view taken along line I-I of Fig. 30[.];

Fig. 32 is a plan view showing the structure of a common contact hole and another gate electrode; and

Fig. 33 is a sectional view taken along line E-E in Fig. 32.--

Paragraph beginning on Page 9, line 12

--The equivalent circuit diagram of Fig. 3 will next be described. Since the transistor Tr is formed in the portion where the gate electrode 30 and the device area overlap one another, the gate electrode 30, first and second diffused layers 20, 21, and well area 10 correspond to gate terminal G, source terminal S, drain terminal D, and substrate B of the transistor, respectively. The gate terminal G and source terminal S are electrically connected with the metal which covers the common contact [60] 80. A parasitic capacitance exists between these terminals by coupling. That is, there are a capacitance Cgs drain between gate and source, a capacitance Cgd between gate and drain, a capacitance Cgb between gate and substrate, a capacitance Csb between source and substrate, and a capacitance Cdb between drain and substrate. Note that since the source terminal S and drain terminal D correspond to the impurity-diffused layers 20 and 21

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which have the same structure, respectively, these terminals do not need to be especially distinguished.--

Paragraph beginning on Page 10, line 7

--Therefore, only the film thickness of the gate insulating film 40 in the common contact hole may be reduced as compared to that of the gate insulating film of the other typical transistors (see Fig. 32 and 33). Moreover, the gate insulating film 40 may be formed with a material having a high dielectric constant. The relative dielectric constant of gate insulating film 40 formed with normal silicon oxide SiO_2 is about 3.8. Examples of a material having a higher relative dielectric constant than 3.8 are titanium oxide and tantalum oxide. Since the capacitance Cgb between gate and substrate is proportional to the relative dielectric constant of the insulating film 40, the additional capacitance may be increased by applying the insulating film 40 having a high dielectric constant only for the common contact [60] 80 portion.--

Paragraphs on Page 11, line 12 through line 21

--In addition, there exists the advantage that using the material having a high dielectric constant only to the insulating film 40 within the common contact hole 60 not only can increase the additional capacitance, but also can suppress the increase of the delay of the transistor for switching.

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In addition, there exists the advantage that increasing the impurity concentration of the first diffused layer 20 within the common contact hole 60 not only can increase the additional capacitance, but also can suppress the increase of the delay of the transistor for switching.--

Page 13, Paragraph Beginning at Line 26

As mentioned above, according to Embodiment 4, [sicne] since the connection is done by both the common contact hole 60 and diffused layer 20, the variation of resistance value may be suppressed.

Marked-up Claims 4, 6, 7, 10, 11 and 13

4. (Amended) A semiconductor device, comprising:

a gate electrode formed on a substrate through a gate insulating film;

a diffused layer formed on the substrate;

a wiring layer formed above the gate electrode; and

a contact formed within a contact hole between the wiring layer and the substrate, which connects the wiring layer to the diffused [layers] layer and the gate electrode,

wherein the diffused layer has first and second portions formed opposite to each other across the portion of the substrate existing under the gate electrode and having a first conduction type, each having a second conduction type different from the first conduction type of the portion of the substrate; and a third portion that connects the first portion to the second portion.

6. (Amended) A semiconductor device according to claim 4, comprising:

another diffused layer formed on the substrate; and

an isolation area formed between the diffused layer and [the] said other diffused layer, which separates the diffused layer and the other diffused layer, wherein the contact is connected further to the other diffused layer.

7. (Amended) A semiconductor device according to claim 1, comprising a SRAM cell, wherein the wiring layer is connected to [the] a memory node of the SRAM cell.

Marked-up Claims 4, 6, 7, 10, 11 and 13

10. (Amended) A semiconductor device according to claim 1, comprising another gate electrode formed on the substrate through another gate insulating film, and a transistor for composing a semiconductor IC therein, wherein the relative dielectric constant of the gate insulating film is higher than the one of [the other] said another gate insulating film.

11. (Amended) A semiconductor device according to claim 1, comprising a source area and a drain area formed opposed to each other across [the] a channel portion of the substrate existing under the gate electrode, and a transistor for composing a semiconductor IC therein, wherein the impurity concentrations of the first diffused layer and the second diffused layer are higher than the ones of the source and the drain areas.

13. (Twice Amended) A semiconductor device according to [claim 1 or] claim 4, comprising a SRAM cell, wherein the wiring layer is connected to [the] a memory node of the SRAM cell.